

Winter Semester 2024-2025

MVLD505P – ASIC Design

SLOT: L23+L24

Submitted to School of Electronics Engineering

Submitted by:

Name: CJ kiran

Reg no: - 24MVD0166

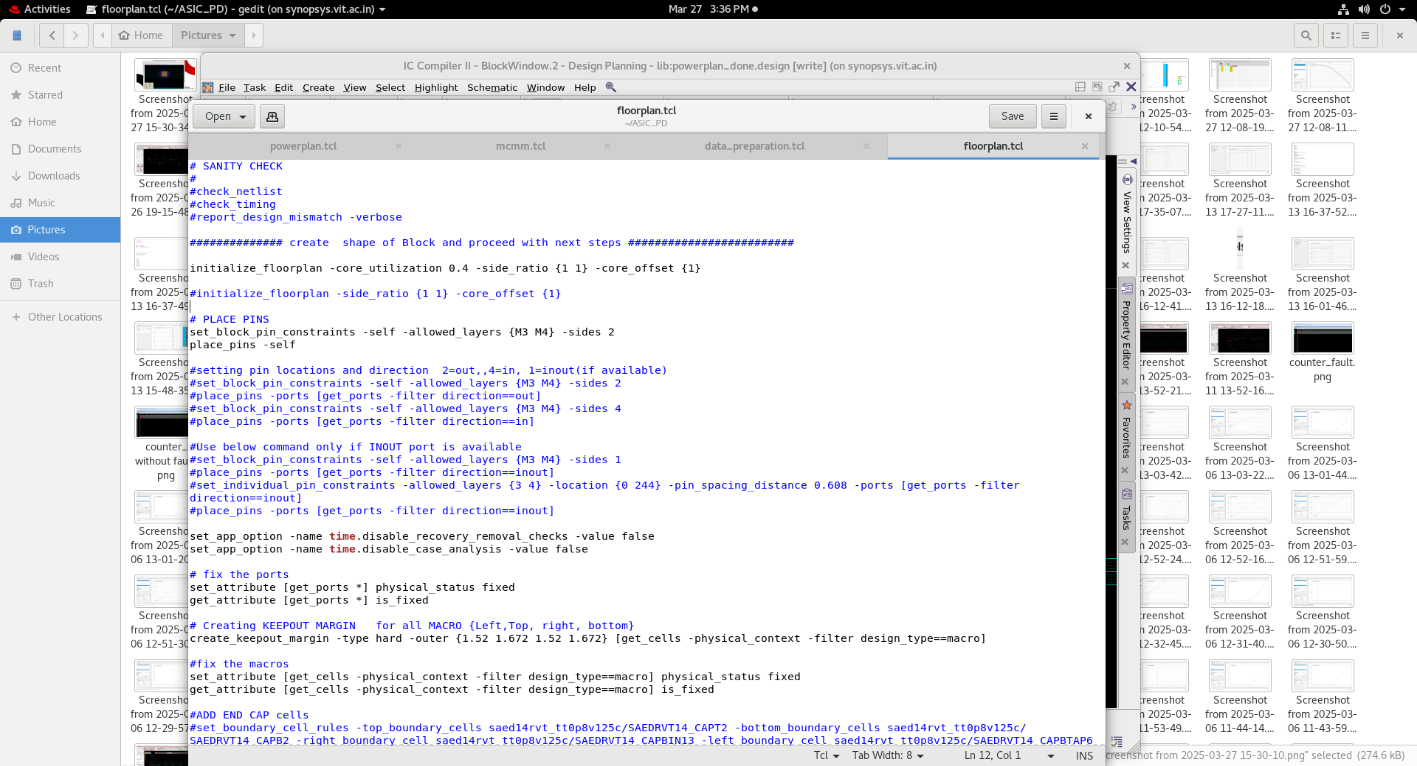
**TASK 4:- ASIC Physical Design Flow**,- **Floorplanning and Power Planning**

**Introduction**

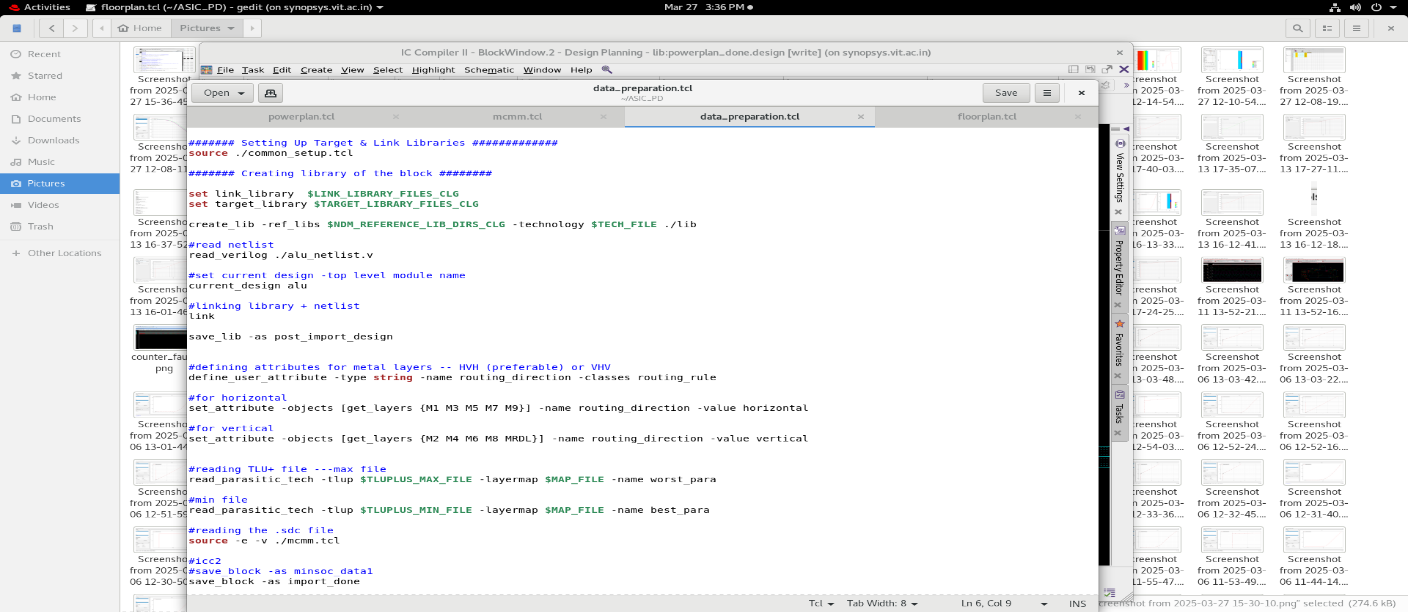
In the **ASIC Physical Design Flow**, **Floorplanning and Power Planning** are crucial steps that significantly impact the chip’s performance, power efficiency, and manufacturability. These steps define the **physical arrangement of components**, ensure optimal connectivity, and establish a robust **power distribution network** to prevent power-related issues.

perform **Floorplanning and Power Planning** using **Synopsys IC Compiler II**.

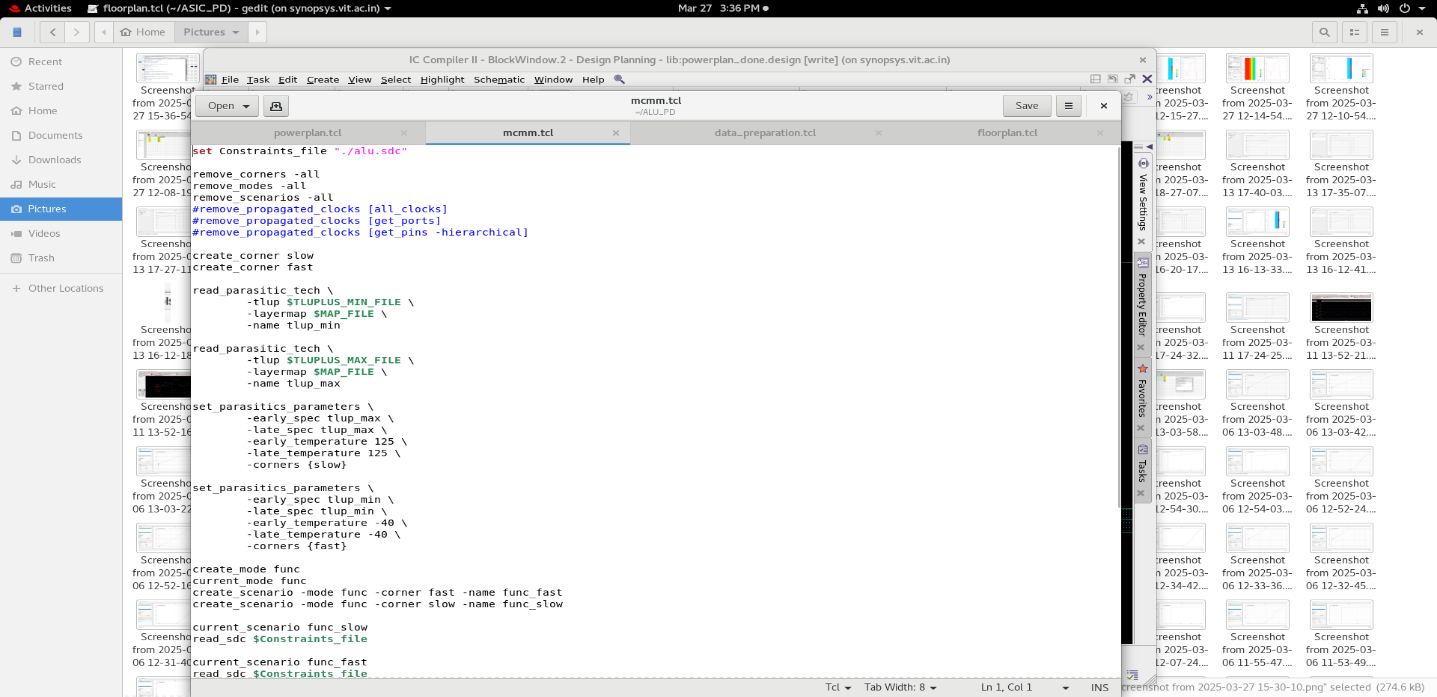
**Floorplan.tcl**



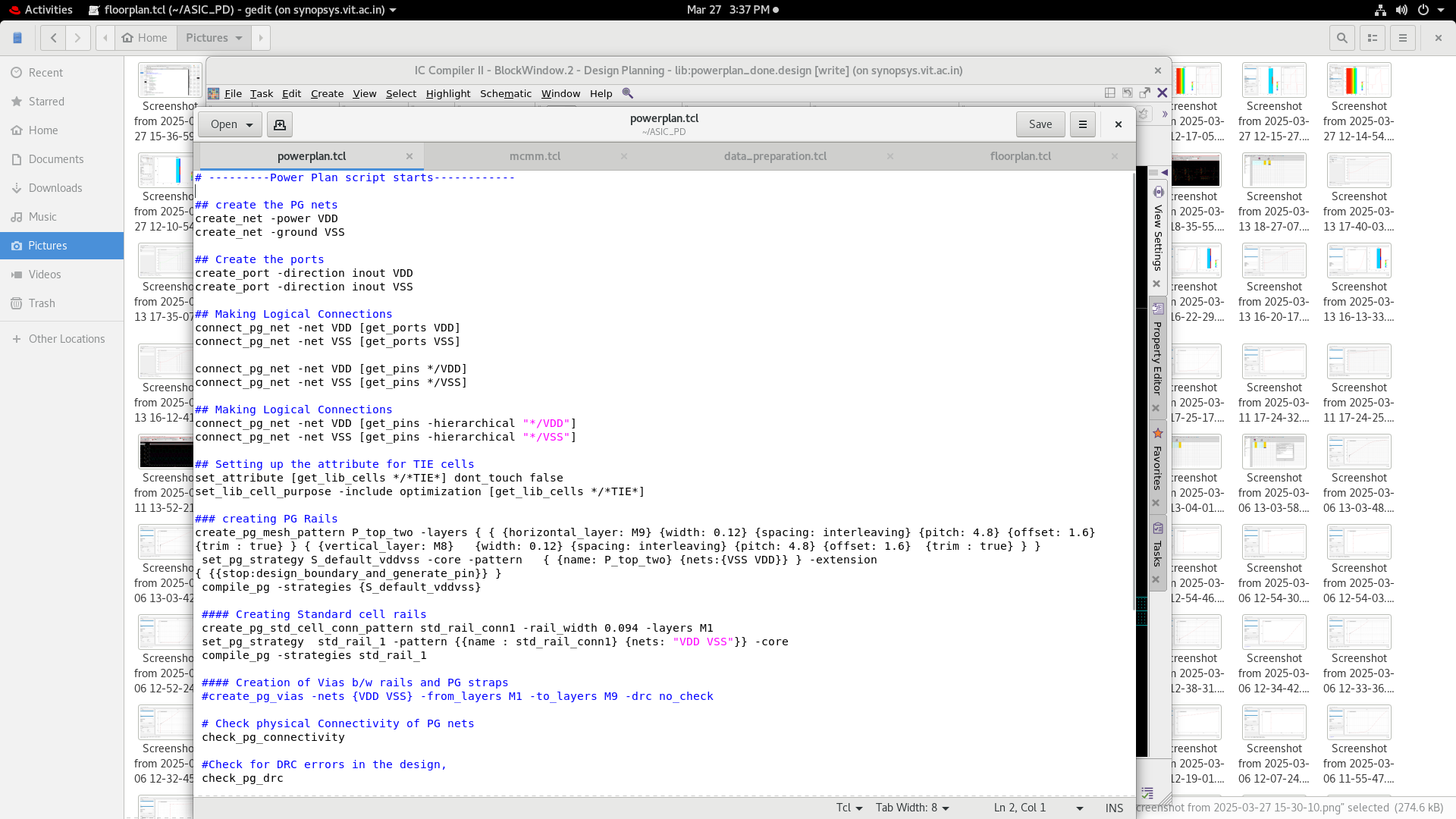
**Data\_preparation.tcl**



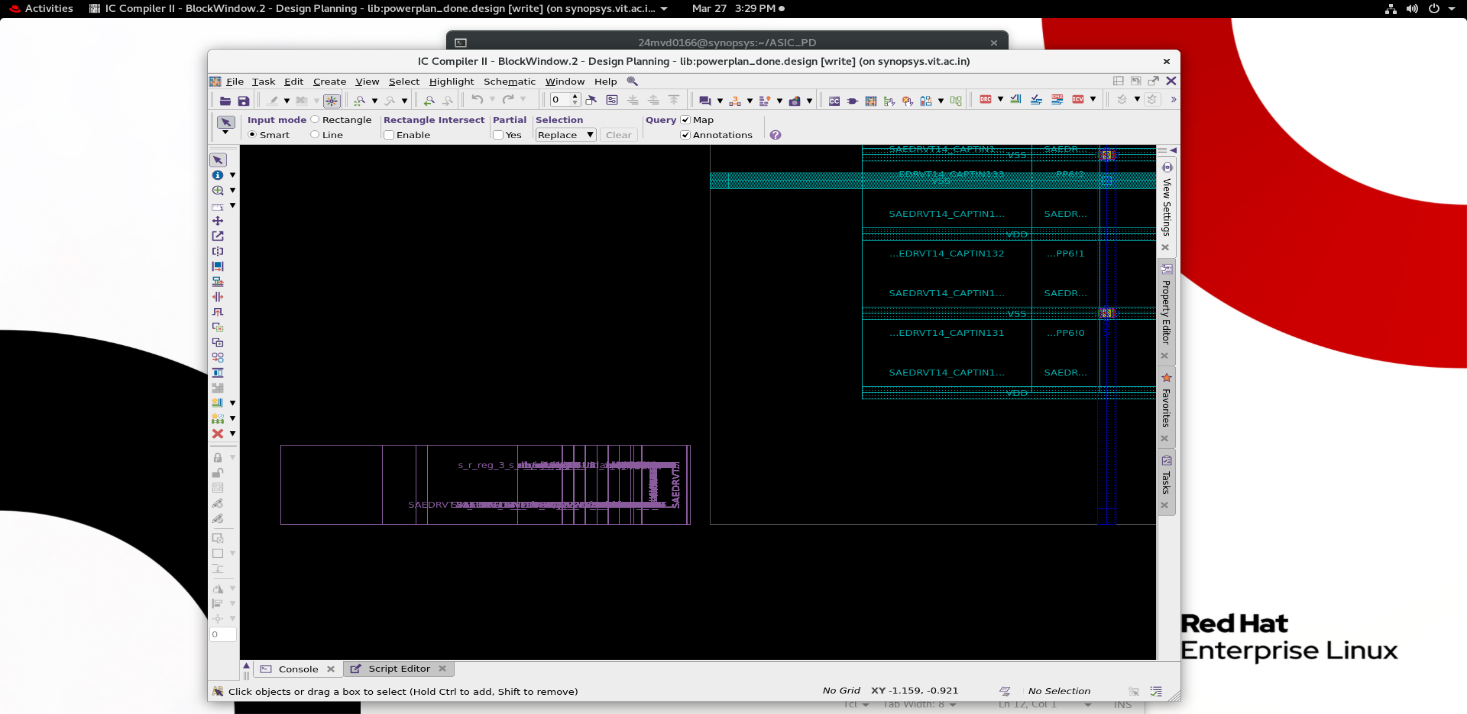
**MCMM.tcl- MCMM (Multi-Corner Multi-Mode) Analysis**



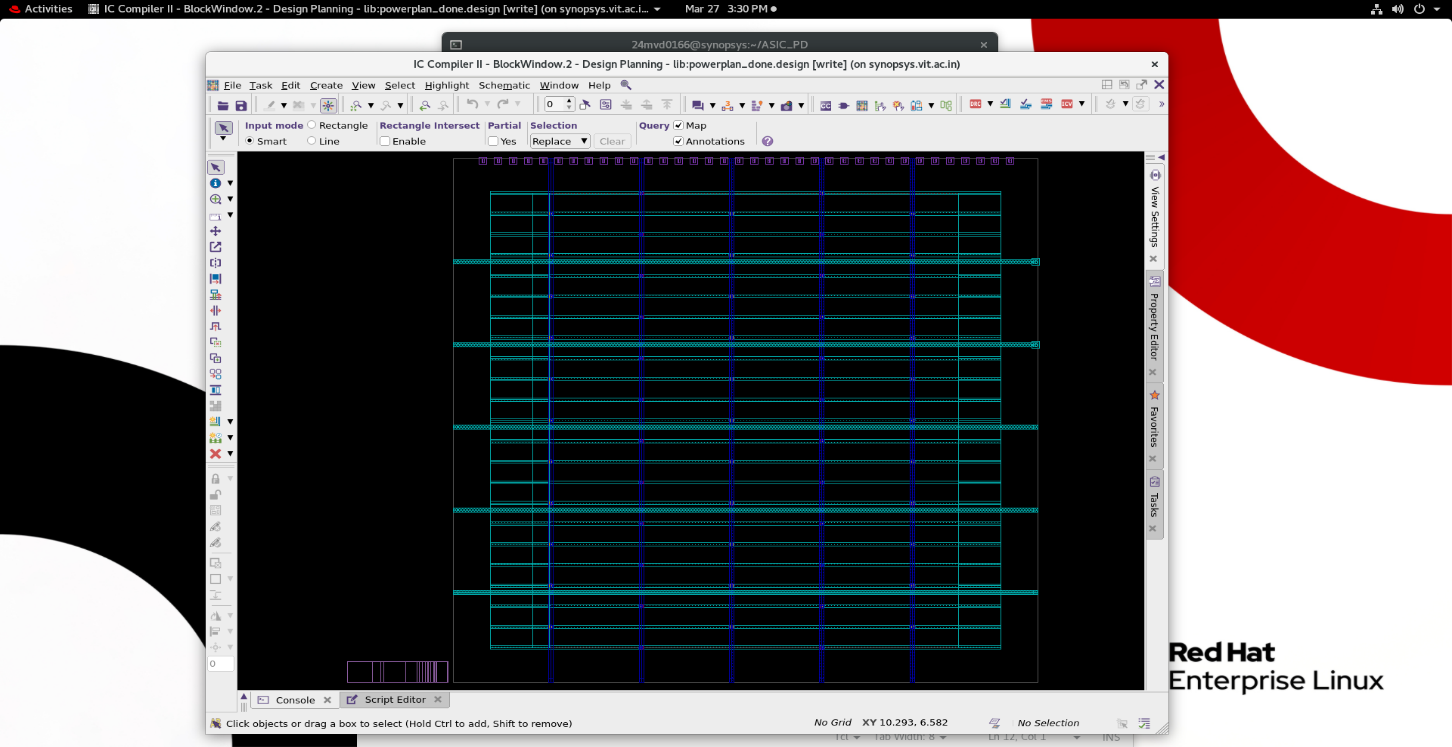
**Powerplan.tcl**



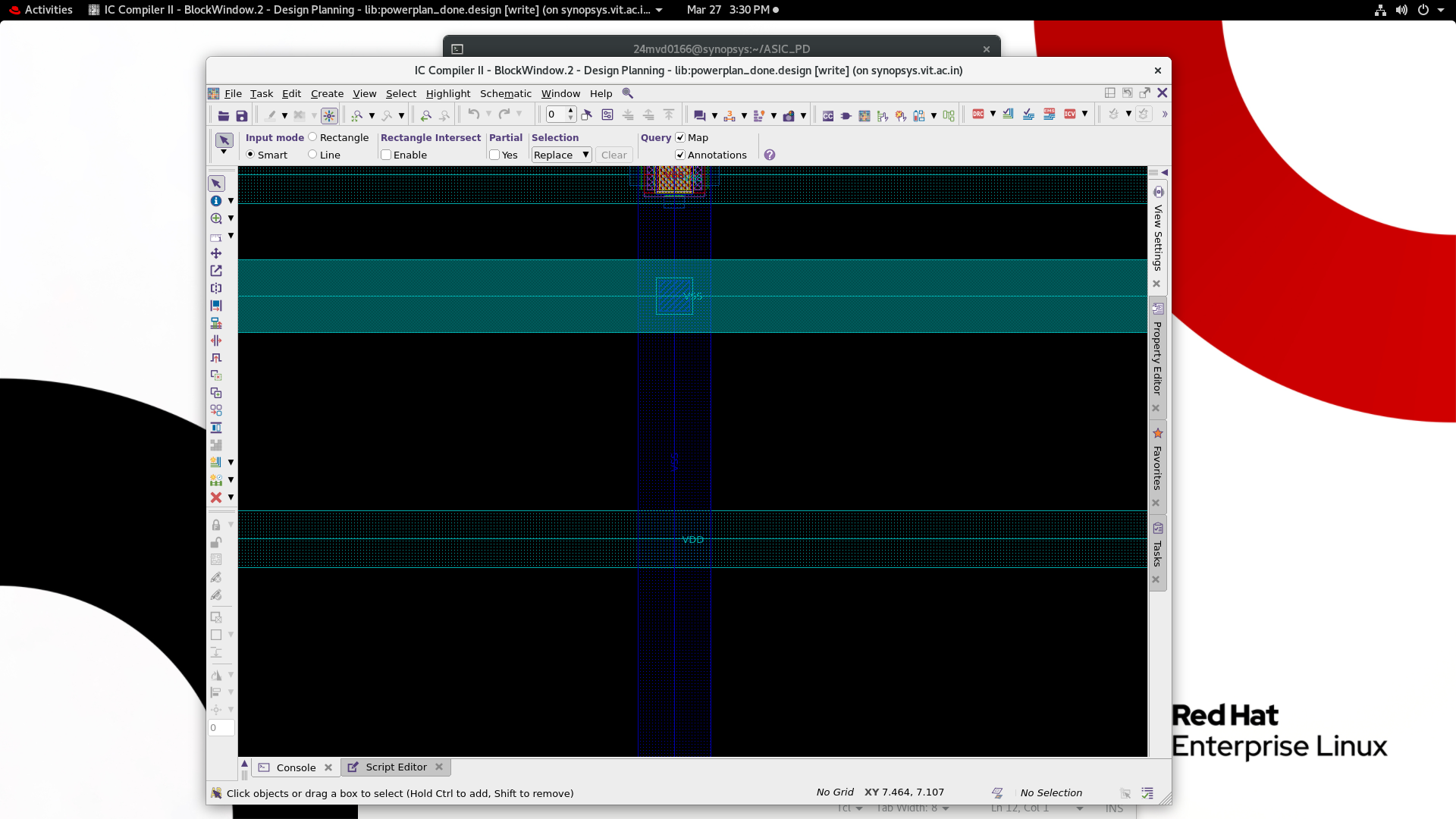
**Standard Cells-** Standard cells are pre-designed logic gates,(ALU block) used to build an ASIC. They are placed in rows inside the core area and connected during placement and routing.



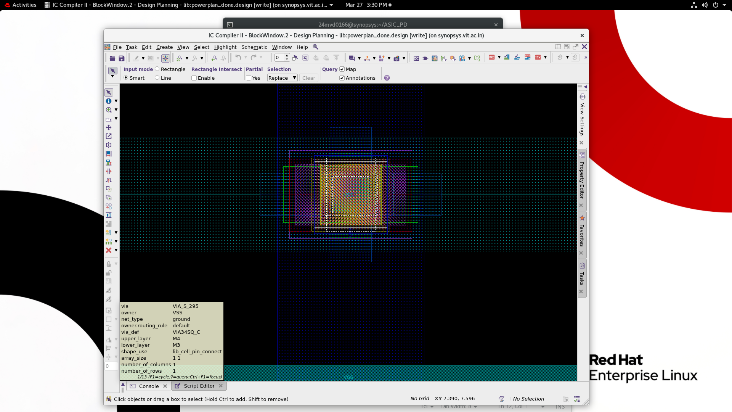
**Floorplan**



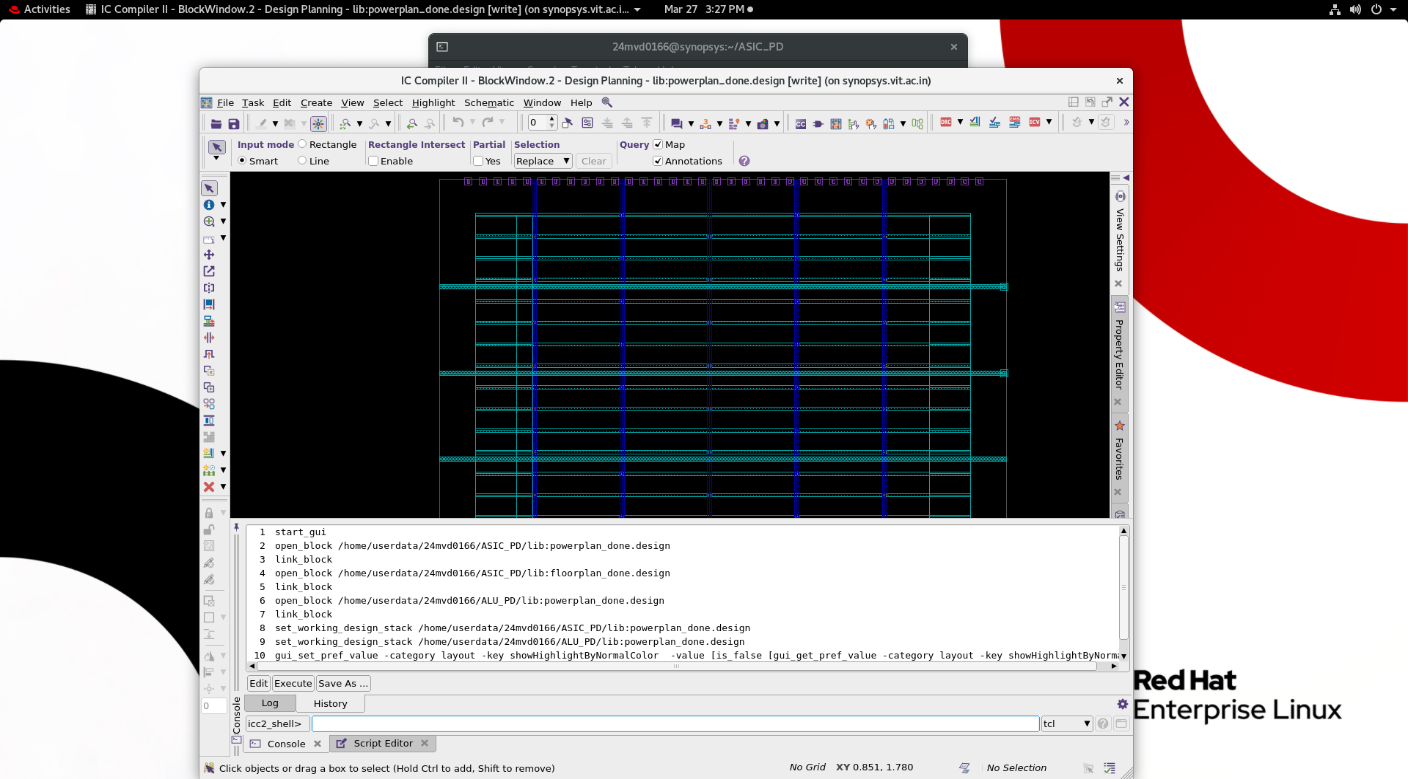
**VSS and VDD**



**Via Block shows the vss and vdd paths**



**Floorplanning and Power Planning- log**



**Conclusion**

**Floorplanning for ALU Design**:

* Organizes **functional blocks** like adders, multiplexers, and logic units efficiently.
* **Optimizes area and timing** to reduce critical path delays.
* Minimizes **routing congestion** by placing frequently interacting blocks close together.

**Power Planning for ALU Design**:

* Ensures **stable power delivery** to high-switching blocks (e.g., adder, shifter).
* Implements **power rings and stripes** to minimize **IR drop and electromigration**.
* Uses **dynamic and leakage power optimization techniques** for better efficiency.

These steps are **critical** before proceeding with **placement, clock tree synthesis (CTS), and routing**, ensuring that the **ALU operates efficiently at all process corners and power modes**.